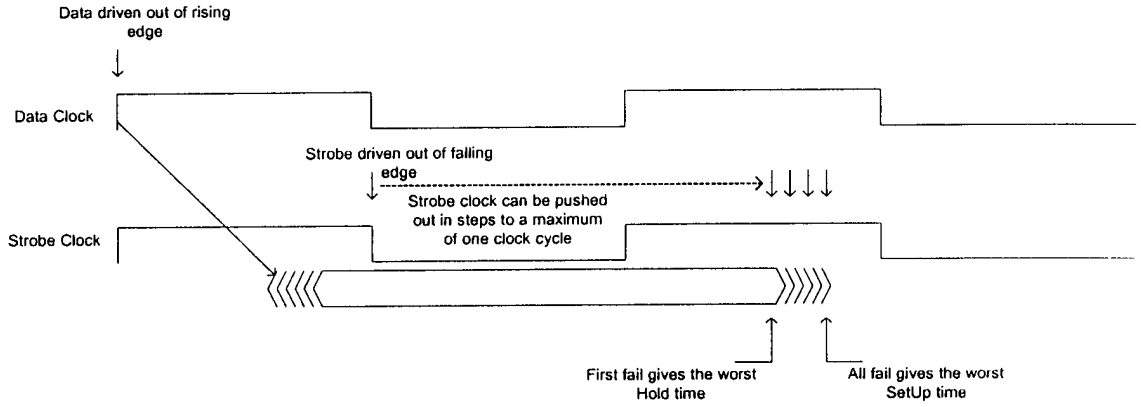

Figure-1. Current methodology. Measuring the setup and hold margins from the trail edge.

The clock supplied to data and strobe clock-macros has to be separated to accommodate the delay

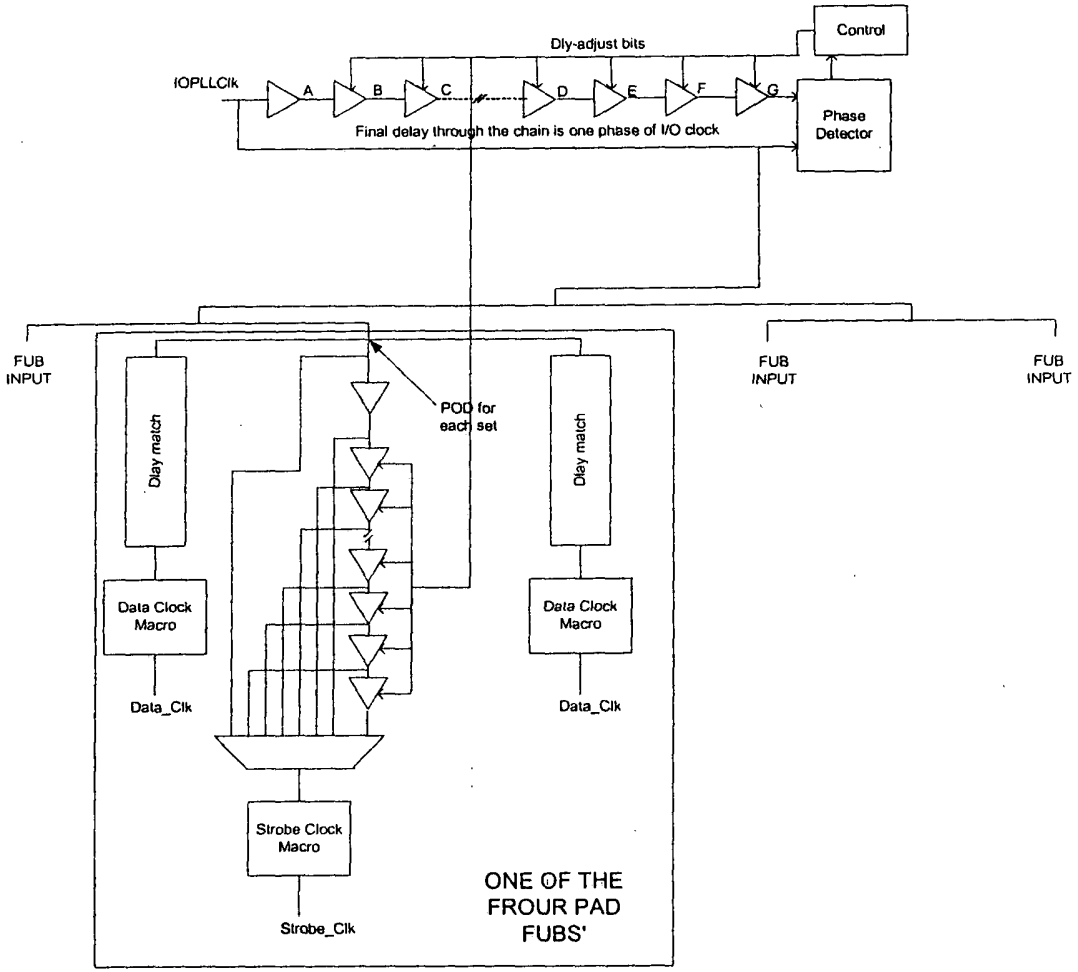

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Figure-2. Implementation of IO Loop-Back mechanism

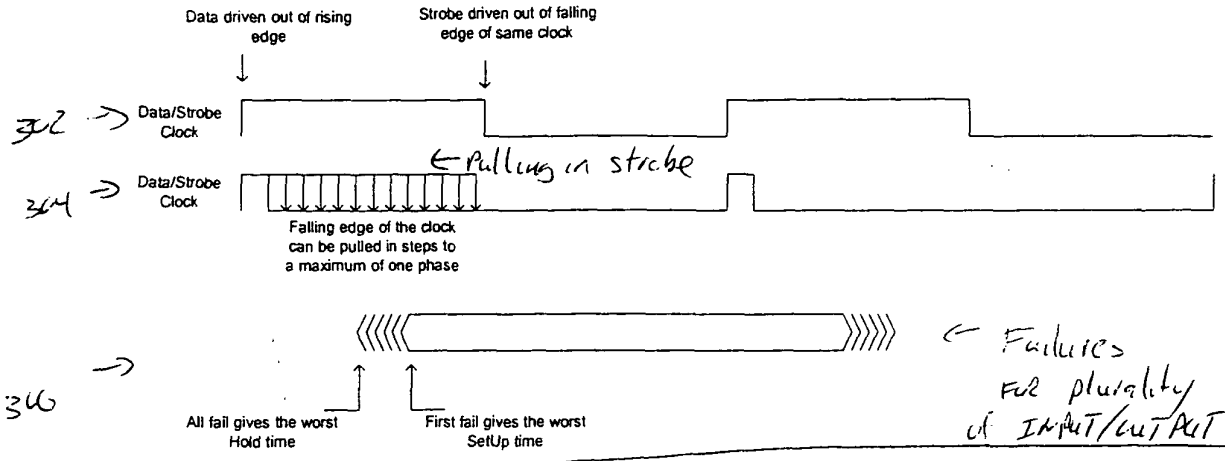


Figure-3. Measuring the setup and hold margins from the lead edge.

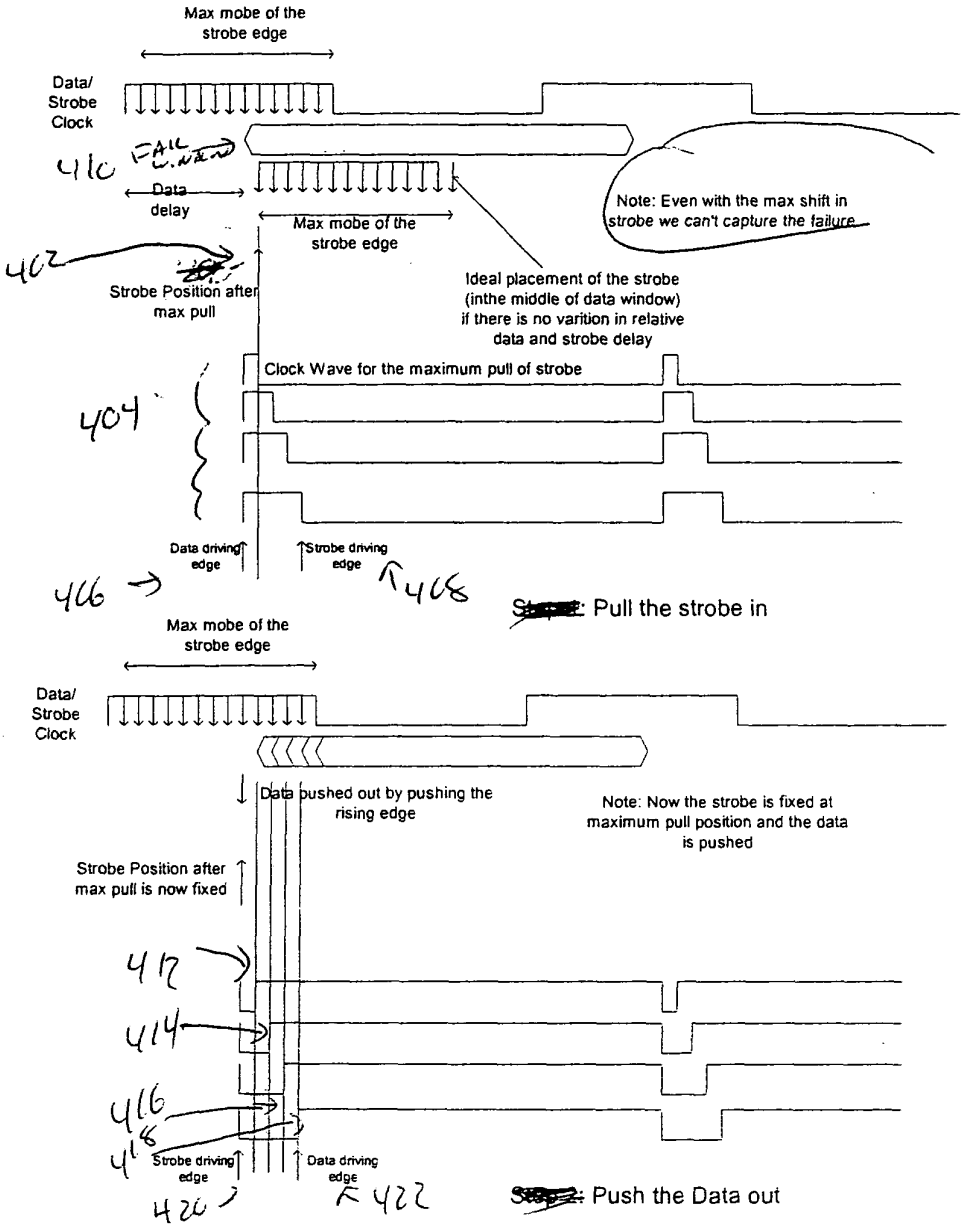


Figure-4. Strobe pull and data push to cover the entire fail window.

Figure-5 and Figure 6 show the

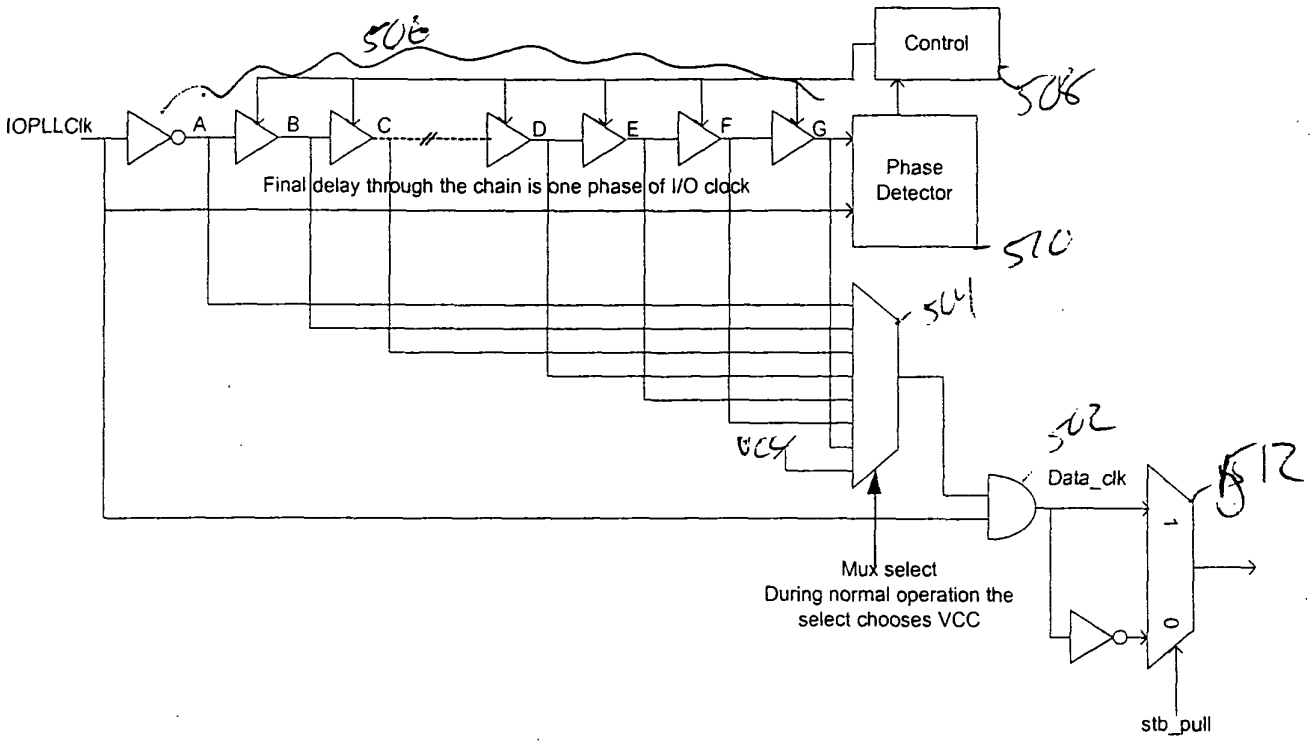


Figure-5. Varying Duty Cycle Clock Generation for strobe pull and data push.

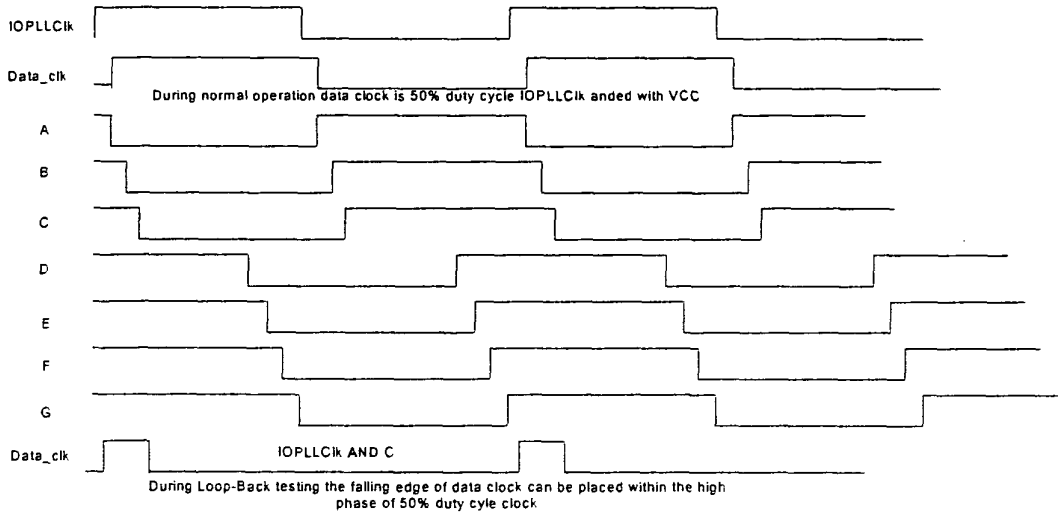
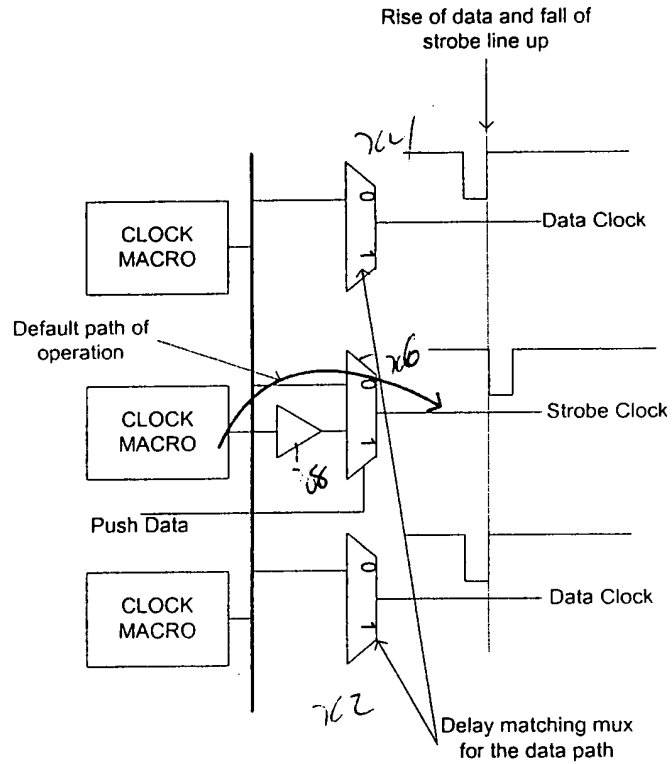


Figure-6. Timing diagram of the delay line and the generation of the non-50% duty cycle data clock

The Data_Clk (varying duty cycle clock

Fig. 7



another embodiment

...h phase to gain higher measurement

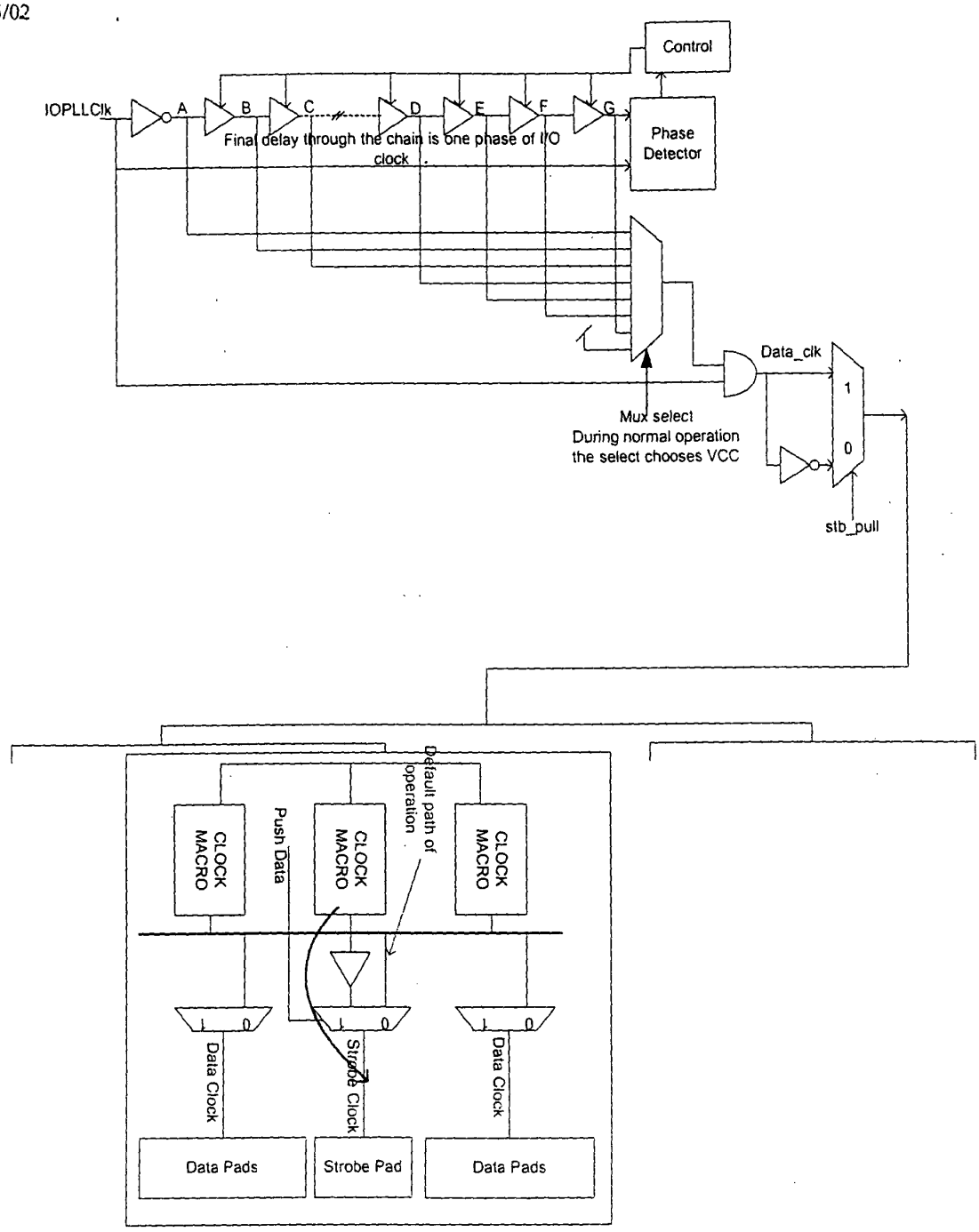


Figure-8. Data and strobe clock distribution per set. Data clock macro inputs and outputs can now be shorted to achieve low skew per set